Agilent HSDL-3202 IrDA® Data 1.3 Low Power Compliant 115.2 Kb/s Infrared Transceiver

Data Sheet

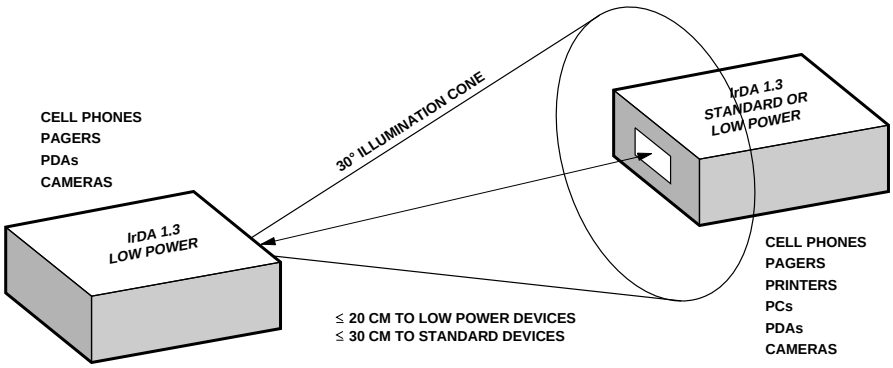
Description

The HSDL-3202 is a new generation of low-cost Infrared (IR) transceiver modules from Agilent Technologies. It features one of the smallest footprints in the industry at 2.5 H x 8.0 W x 3.0 D mm. Although the supply voltage can range from 2.7 V to 3.6 V, the LED drive current is internally compensated to a constant 32 mA to guarantee link distance of IrDA Data 1.3 (low power) physical layer specification.

The HSDL-3202 meets the link distance of 20 cm to other IrDA 1.3 low power devices, and 30 cm to standard one meter IrDA 1.3 devices. It is designed to interface to input/output logic circuits as low as 1.8 V.

Features

- **Ultra small surface mount package**
- **Minimal height: 2.5 mm**
- **V_{CC} from 2.7 to 3.6 volts**
- **Interface to input/output logic circuits as low as 1.8 V**
- **LED supply voltage can range from 2.7 to 6 volts**
- **Low I_{CC} shutdown current**
  – 10 nA typical
- **Complete shutdown**
  – TxD, RxD, PIN diode
- **Three optional external components**
- **Temperature performance guaranteed, –25°C to 85°C**
- **32 mA LED drive current**
- **Integrated EMI shield**
- **IEC825-1 class 1 eye safe**
- **Edge detection input**
  – prevents the LED from long turn on time



Applications

- **Mobile telecom**
  – cellular phones
  – pagers
  – smart phones
- **Data communication**
  – PDAs
  – portable printers
- **Digital imaging**
  – digital cameras
  – photo-imaging printers
- **Electronic wallet**

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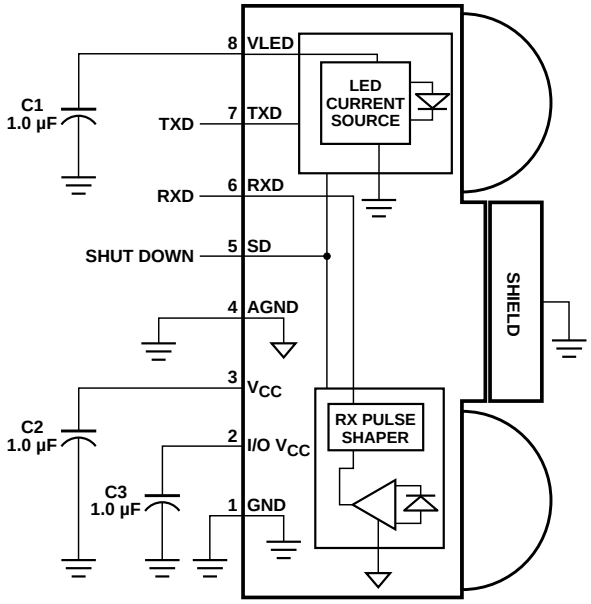
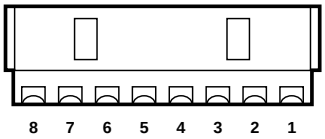
Application Circuit



Pinout, Rear View



I/O Pins Configuration Table

Pin	Symbol	Description	Notes
1	GND	Ground	Connect to system ground
2	IOV_{CC}	Input/Output ASIC V_{CC}	Connect to ASIC logic controller V_{CC} voltage
3	V_{CC}	Supply Voltage	Regulated, 2.7 to 3.6 volts
4	AGND	Analog Ground	Connect to a "quiet" ground
5	SD	Shut Down Active High	This pin must be driven either high or low. Do NOT float the pin.
6	RXD	Receiver Data Output Active Low	Output is a low pulse for 1.6 µs when a light pulse is seen
7	TXD	Transmitter Data Input Active High	Logic High turns on the LED. If held high longer than ~ 20 µs, the LED is turned off. TXD must be driven high or low. Do NOT float the pin.
8	VLED	LED Supply Voltage	May be unregulated, 2.7 to 6 volts.
–	SHIELD	EMI Shield	Connect to system ground via a low inductance trace. For best performance, do not connect to GND or AGND directly at the part.

Recommended Application Circuit Components

Component	Recommended Value	Note
C1	1.0 µF, ± 20%, Tantalum	1
C2	1.0 µF, ± 20%, Tantalum	1
C3	1.0 µF, ± 20%, Tantalum	1

Absolute Maximum Ratings

For implementations where case-to-ambient thermal resistance is ≤ 50°C/W.

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	–40	100	°C
Operating Temperature	T_A	–25	85	°C
LED Supply Voltage	V_{VLED}	0	7	V
Supply Voltage	V_{CC}	0	7	V
Input/Output Voltage	IOV_{CC}	0	7	V
Input Voltage: TXD, SD	V_I	0	IOV_{CC} + 0.5	V
Output Voltage: RXD	V_O	–0.5	IOV_{CC} + 0.5	V
Solder Reflow Temperature Profile		See page 12		

Transceiver I/O Truth Table

The outputs (LED and RXD) are controlled by the combination of the TXD and SD (shutdown) pins and light falling on the receiver. As shown in the table below, the transmitter is non-inverting; the LED is on when the TXD pin is high and off when TXD is low.

The receiver is inverting; the RXD pin is low during IrDA signal pulses and high when the receiver does not see any light. When shutdown (SD pin high), the LED is off (the state of the TXD pin does not matter), and the RXD pin is pulled high with a weak internal pullup.

SD	TXD	LED	Receiver	RXD	Notes
Low	High	On	Don't care	Not valid	2
	Low	Off	IrDA signal	Low	3, 4
			No signal	High	
High	Don't care	Off	Don't care	High	5

Shutdown Mode Notes

When the HSDL-3202 is in Shutdown Mode (SD pin high), the part presents different impedances to the rest of the circuit than when it is in normal mode.

RXD Pin: This pin is NOT Tri-state. During shutdown the equivalent circuit is a weak pullup (~300 kΩ) to V_{CC}. The ESD protection diodes to V_{CC} and Ground are also present.

TXD Pin: Input protection diodes are present.

VLED Pin: Typical leakage current of 1.5 nA.

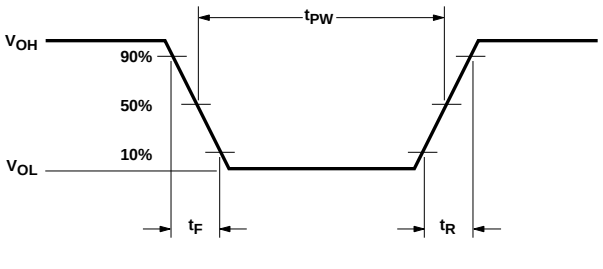
SD Pin: Will draw approximately 10 nA when driven high.

Caution: The BiCMOS inherent to this design of this component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

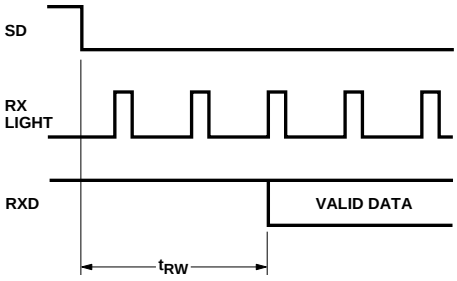
Recommended Operating Conditions

Parameter		Symbol	Min.	Max.	Units	Conditions	Notes
Operating Temperature		T_A	–25	85	°C		
Supply Voltage		V_{CC}	2.7	3.6	V		
Input/Output Voltage		IOV_{CC}	1.8	V_{CC}	V	IOV_{CC} operational at 1.5 V at reduced spec	
LED Supply Voltage		V_{LED}	2.7	6	V		
TXD, SD Input Voltage	Logic High	V_{IH}	2/3 IOV_{CC}	IOV_{CC}	V	$IOV_{CC} \geq 1.8$ V	
	Logic Low	V_{IL}	0	1/3 IOV_{CC}	V	$IOV_{CC} \geq 1.8$ V	
Receiver Input Irradiance	Logic High	EI_H	0.0081	500	mW/cm^2	For in-band signals	7
	Logic Low	EI_L		0.4	μW/cm^2	For in-band signals	7
Receiver Data Rate			2.4	115.2	Kb/s		
Ambient Light				See Test Methods on page 15 for details			

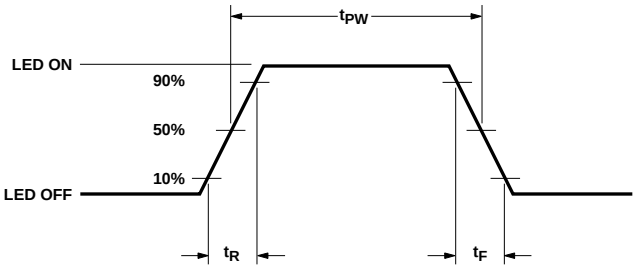
RXD Output Waveform



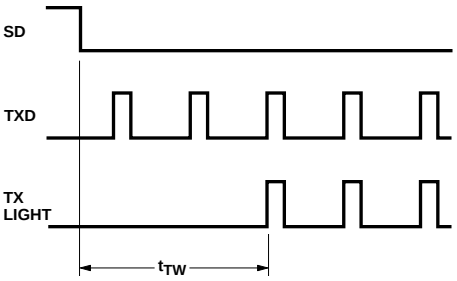
Receiver Wakeup Time Definition



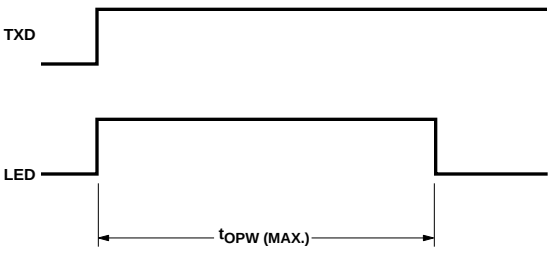
LED Optical Waveform



Transmitter Wakeup Time Definition



TXD "Stuck ON" Protection



Electrical & Optical Specifications

Specifications hold over the recommended operating conditions unless otherwise noted. Unspecified test conditions may be anywhere in their operating range. All typical values are at 25°C and 3.0 V unless otherwise noted.

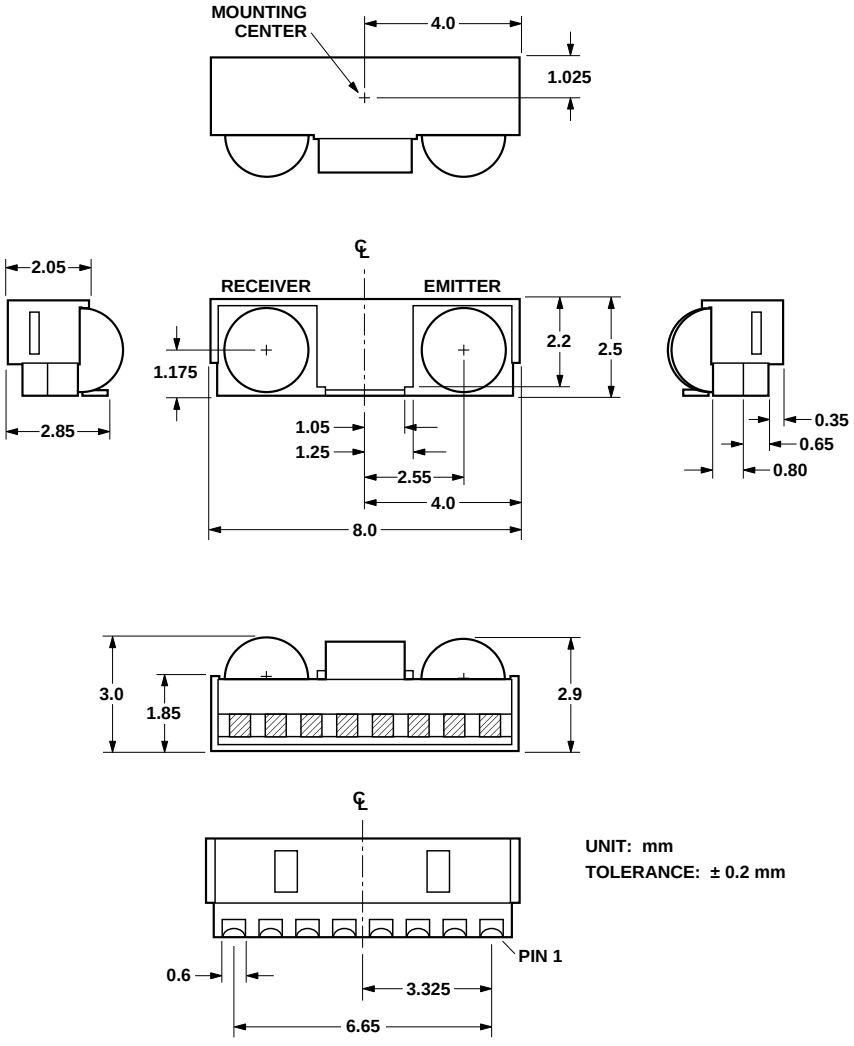
Parameter		Symbol	Min.	Typ.	Max.	Units	Conditions	Note
Receiver								
Viewing Angle		$2\theta_{1/2}$	30	–	–	°		
Peak Sensitivity Wavelength		λp	–	880	–	nm		
RXD Output Voltage	Logic High	V_{OH}	$IOV_{CC} - 0.2$	–	IOV_{CC}	V	$I_{OH} = -200\ \mu A$, EI ≤ 0.3 μW/cm²	
	Logic Low	V_{OL}	0	–	0.3	V	$I_{OL} = 200\ \mu A$	7
RXD Pulse Width		t_{PW}	–	2.5	3.5	μs		7
RXD Rise Times		t_R	–	20	70	ns	t_{PW} (EI) = 1.6 μs, C_L = 9.0 pF Max. value @ IOV_{CC} = 1.8 V	
RXD Fall Times		t_F	–	25	50	ns	t_{PW} (EI) = 1.6 μs, C_L = 9.0 pF	
Receiver Latency Time		t_L	–	20	50	μs		8
Receiver Wake Up Time		t_{RW}	–	20	100	μs		9
Transmitter								
Radiant Intensity		IE_H	4	8	28.8	mW/Sr	T_A = 25°C, $\theta_{1/2} \leq 15°$, TXD ≥ 2/3 IOV_{CC}	
Viewing Angle		$2\theta_{1/2}$	30	–	60	°		
Peak Wavelength		λ_p	–	875	–	nm		
Spectral Line Half Width		$\Delta\lambda_{1/2}$	–	35	–	nm		
Optical Pulse Width		t_{OPW}	–	2.0	2.23	μs	t_{PW} (TXD) = 1.6 μs	
			–	20	30	μs	TXD pin stuck high	
Optical Rise and Fall Times		t_{OR}	–	–	600	ns	t_{PW} (TXD) = 1.6 μs	
Optical Rise and Fall Times		t_{OF}	–	–	600	ns	t_{PW} (TXD) = 1.6 μs	
TXD Logic Levels	High	V_{IH}	2/3 IOV_{CC}	–	IOV_{CC}	V	$IOV_{CC} \geq 1.8$ V	
	Low	V_{IL}	0	–	1/3 IOV_{CC}	V	$IOV_{CC} \geq 1.8$ V	
TXD Input Current	High	I_H	–	0.01	1	μA	$V_I \geq 2/3\ IOV_{CC}$	
	Low	I_L	–1	-0.01	–	μA	$0 \leq VI \leq 1/3\ IOV_{CC}$	
LED Current	On	I_{VLED}	–	32	38	mA	$V_{VLED} = V_{CC}$ = 3.6 V, V_I(TXD) ≥ 2/3 IOV_{CC}	
	Off	I_{VLED}	–	0.0015	1	μA	$V_{VLED} = V_{CC}$ = 3.6 V, V_I(TXD) ≤ 1/3 IOV_{CC}	
	Shutdown	I_{VLED}	–	0.0015	1	μA	V_I(SD) ≥ 2/3 IOV_{CC}	
Transmitter Wake Up Time		t_{TW}	–	12	100	μs		10

Parameter		Symbol	Min.	Typ.	Max.	Units	Conditions	Note
Transceiver								
SD Logic Levels	High	V_{IH}	2/3 IOV_{CC}	–	IOV_{CC}	V	$IOV_{CC} \geq 1.8$ V	
	Low	V_{IL}	0	–	1/3 IOV_{CC}	V	$IOV_{CC} \geq 1.8$ V	
SD Input Current	High	I_H	–	10	200	nA	$V_I \geq 2/3\ IOV_{CC}$. Max value at 25°C	
	Low	I_L	–300	–10	–	nA	$0 \leq V_I \leq 1/3\ IOV_{CC}$. Max value at 25°C	
Supply Current	Shutdown	I_{CC1}	–	10	200	nA	V_{CC} = 3.6 V, $V_{SD} = IOV_{CC}$	
	Idle	I_{CC2}	–	100	250	µA	V_{CC} = 3.6 V, V_I(TXD) ≤ 1/3 IOV_{CC}, EI=0	
	Peak Active Receive	I_{CC3}	–	2.0	10.0	mA	V_{CC} = 3.6 V, V_I(TXD) ≤ 1/3 IOV_{CC}	11, 12
	Peak Active Transmit	I_{CC4}	–	5.0	9.0	mA	V_{CC} = 3.6 V, V_I(TXD) ≤ 2/3 IOV_{CC}	11
IOV_{CC} Current		$I_{IOV_{CC}}$	–	30	200	nA		

Notes:

1. C1,C2, and C3 must be placed within 0.7 cm of the HSDL-3202 to obtain optimum noise immunity. If V_{LED} and V_{CC} are tied together, then the application may use one less capacitor.
2. If TXD is stuck in the high state, the LED will turn off after about 20 µs.
3. In-Band IrDA signals and data rates ≤ 115.2 Kb/s.
4. RXD Logic Low is a pulsed response. The condition is maintained for a duration that is dependent upon the data pattern.
5. RXD Logic High during shutdown is a weak pullup resistor (300 kΩ).
6. An in-band optical signal is a pulse/sequence where the peak wavelength, λ_p, is defined as 850 nm ≤ λ_p ≤ 900 nm, and the pulse characteristics are compliant with the IrDA Serial Infrared Physical Layer Link Specification.
7. For in-band signals [115.2 Kb/s where 8.1 µW/cm^2 ≤ EI ≤ 500 mW/cm^2].
8. Latency is defined as the time from the last TXD light output pulse until the receiver has recovered full sensitivity.
9. Receiver wake up time is measured from the SD pin high-to-low transition or V_{CC} power on to valid RXD output.
10. Transmitter wake up time is measured from the SD pin high-to-low transition or V_{CC} power on to valid light output in response to a TXD pulse.
11. Typical values are at EI = 10 mW/cm^2.
12. Maximum value is at EI = 500 mW/cm^2.

Package Dimensions



Moisture Proof Packaging

The HDSL-3202 is shipped in moisture proof packaging. Once opened, moisture absorption begins.

Recommended Storage Conditions

Storage Temperature	10°C to 30°C
Relative Humidity	below 60% RH

Time from Unsealing to Soldering

After removal from the bag, the parts should be soldered within two days if stored at the recommended storage conditions. If times longer than two days are needed, the parts must be stored in a dry box.

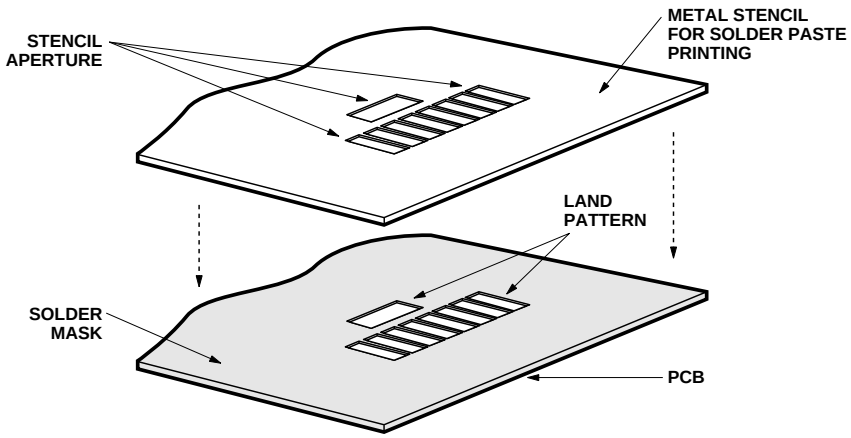
Baking

If the parts are not stored in dry conditions, they must be baked before reflow to prevent damage to the parts.

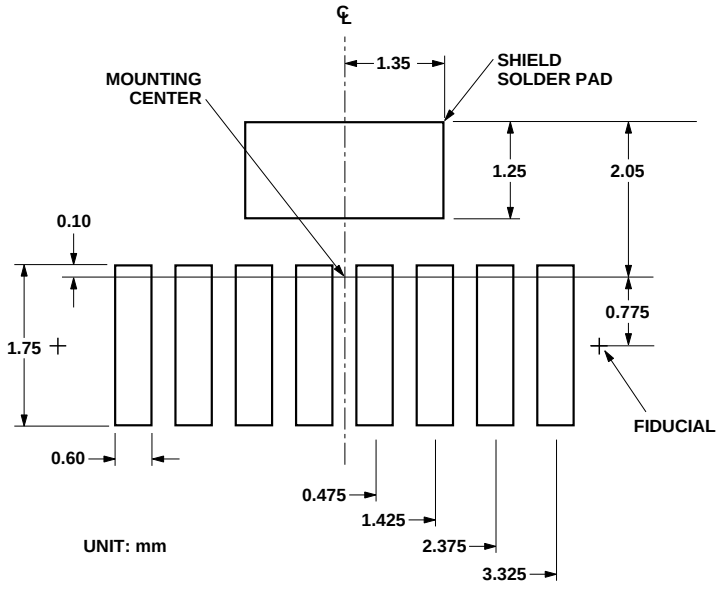
Package	Temp.	Time
In reels	60°C	≥48 hours
In bulk	100°C	≥4 hours
	125°C	≥2 hours
	150°C	≥1 hour

Baking should only be done once.

Solder Pad, Mask and Metal Stencil



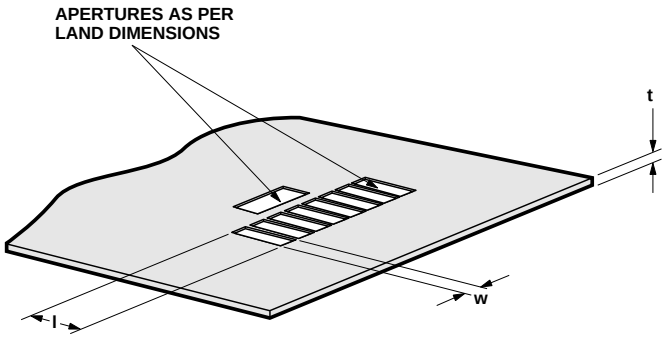
Recommended Land Pattern



Recommended Metal Solder Stencil Aperture

It is recommended that only a 0.152 mm (0.006 inch) or a 0.127 mm (0.005 inch) thick stencil be used for solder paste printing. This is to ensure adequate printed solder paste volume and no shorting. See the table below the drawing for combinations of metal stencil aperture and metal stencil thickness that should be used.

Aperture opening for shield pad is 2.7 mm x 1.25 mm as per land pattern.



Stencil Thickness, t (mm)	Aperture Size (mm)	
	Length, l	Width, w
0.152 mm	2.60 ± 0.05	0.55 ± 0.05
0.127 mm	3.00 ± 0.05	0.55 ± 0.05

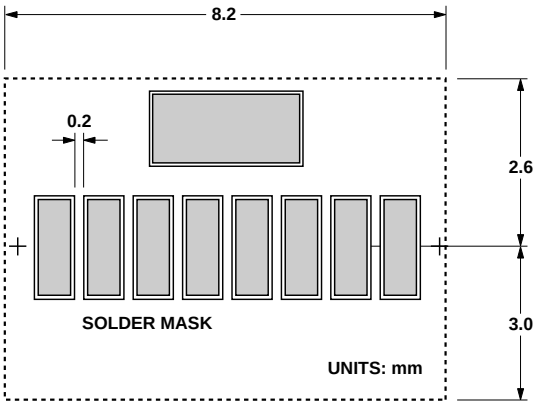
Adjacent Land Keepout and Solder Mask Areas

Adjacent land keepout is the maximum space occupied by the unit relative to the land pattern. There should be no other SMD components within this area.

0.2 mm is the minimum solder resist strip width required to avoid solder bridging adjacent pads.

It is recommended that two fiducial crosses be placed at mid-length of the pads for unit alignment.

Note: Wet/Liquid Photo-Imageable solder resist/mask is recommended.

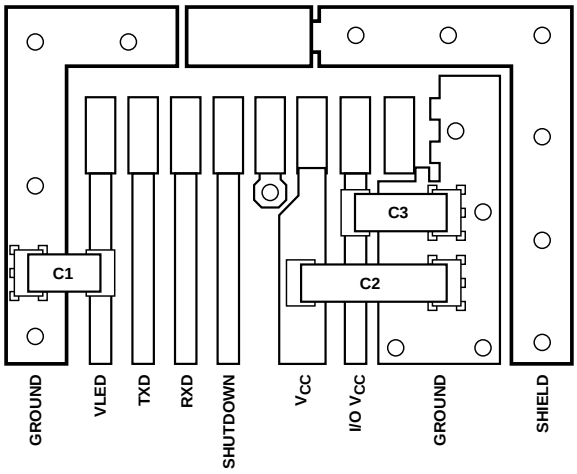


PCB Layout Suggestion

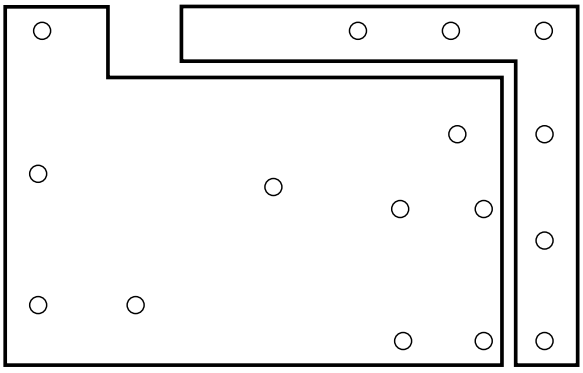
The following PCB layout shows a recommended layout that should result in good electrical and EMI performance. Things to note:

1. The ground plane should be continuous under the part, but should not extend under the shield trace.
2. The shield trace is a wide, low-inductance trace back to the system ground.
3. The AGND pin is connected to the ground plane and not to the shield tab.
4. C1, C2, and C3 are optional supply filter capacitors; it may be left out if the supply is clean.
5. V_{LED} can be connected to either unfiltered or unregulated power. If C1 is used, and if V_{LED} is also connected to V_{CC}, the connection should be before the C1 cap.

Component Side



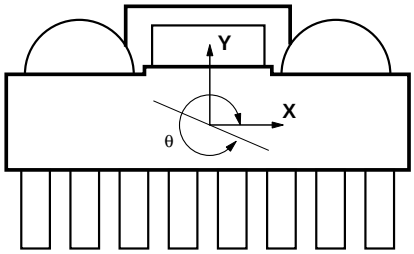
Circuit Side



Pick and Place Misalignment Tolerance and Self-Alignment after Solder Reflow

If the printed solder paste volume is adequate, the HSDL-3202 will self-align after solder reflow. Units should be properly reflowed in IR/hot air convection oven using the recommended reflow profile. The direction of board travel does not matter.

Direction Definition



Allowable Misalignment

Direction	Tolerance
X	≤ 0.2 mm
Y	See text
θ	≤ ± 3 degrees

Tolerance for X-axis Alignment of Castellation

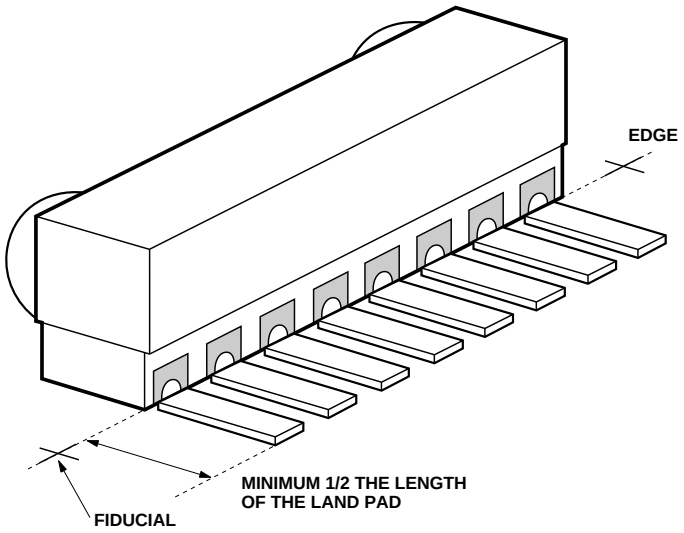
Misalignment of castellation to the land pad should not exceed 0.2 mm or about one-half the width of the castellation during placement of the unit. The castellations will self-align to the pads during solder reflow.

Tolerance for Rotational (θ) Misalignment

Mounted units should not be rotated more than ± 3 degrees with reference to center X-Y as shown in the direction definition. Units that are rotated more than ± 3 degrees will not self-align after solder reflow. Units with less than a ± 3 degree misalignment will self-align after solder reflow.

Y-axis Misalignment of Castellation

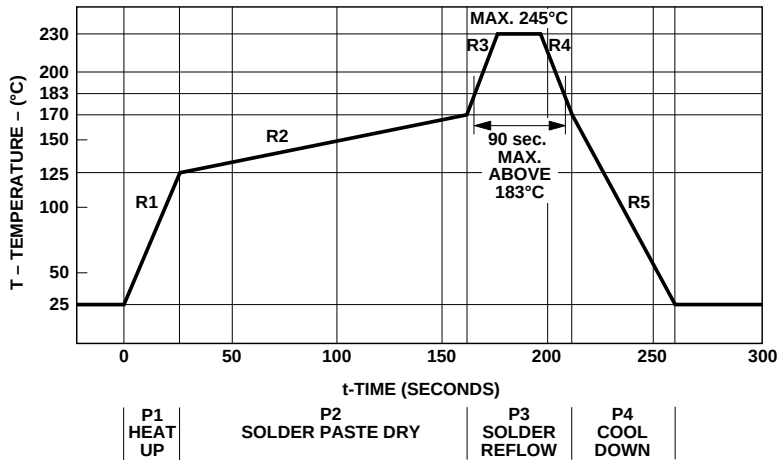
In the Y direction, the HSDL-3202 does not self-align after solder reflow. Agilent recommends that the part be placed in line with the fiducial mark (mid-length of land pad). This will enable sufficient land length (minimum of 1/2 land length) to form a good joint. See the drawing below.



Recommended Solder Paste/Cream Volume for Castellation Joints

Based on calculation and experiment, the printed solder paste volume required per castellation pad is 0.22 cubic mm (based on either no-clean or aqueous solder cream types with typically 60% to 65% solid content by volume). Using the recommended stencil will result in this volume of solder paste.

Reflow Profile



Process Zone	Symbol	ΔT	Maximum ΔT/Δtime
Heat Up	P1, R1	25°C to 125°C	4°C/s
Solder Paste Dry	P2, R2	125°C to 170°C	0.5°C/s
Solder Reflow	P3, R3	170°C to 230°C (245°C max.)	4°C/s
	P3, R4	230°C to 170°C	–4°C/s
Cool Down	P4, R5	170°C to 25°C	–3°C/s

The reflow profile is a straight line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different ΔT/Δtime temperature change rates. The ΔT/Δtime rates are detailed in the above table. The temperatures are measured at the component to printed-circuit board connections.

In **process zone P1**, the PC board and HSDL-3202 castellation I/O pins are heated to a temperature of 125°C to activate the flux in the solder paste. The temperature ramp-up rate, R1, is limited to 4°C per second to allow for even heating of both the PC board and HSDL-3202 castellation I/O pins.

Process zone P2 should be of sufficient time duration (> 60 seconds) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder, usually 170°C (338°F).

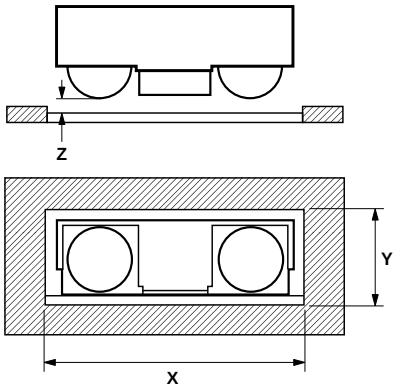
Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 230°C (446°F) for optimum results. The dwell time above the liquidus point of solder should be between 15 and 90 seconds. It usually takes about 15 seconds to assure proper coalescing of the solder balls into liquid solder and the formation of good solder connections. Beyond a dwell time of 90 seconds, the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder, usually 170°C (338°F), to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed –3°C per second maximum. This limitation is necessary to allow the PC board and HSDL-3202 castellation I/O pins to change dimensions evenly, putting minimal stresses on the HSDL-3202 transceiver.

Window Design

To ensure IrDA compliance, some constraints on the height and width of the window exist. The minimum dimensions ensure that the IrDA cone angles are met without vignetting. The maximum dimensions minimize the effects of stray light. The minimum size corresponds to a cone angle of 30 degrees, the maximum to a cone angle of 60 degrees.

The drawing below shows the module positioned in front of a window.



X is the width of the window, Y is the height of the window, and Z is the distance from the HSDL-3202 to the back of the window. The distance from the center of the LED lens to the center of the photodiode lens is 5.1 mm. The equations for the size of the window are as follows:

$X = 5.1 + 2(Z + D) \tan \theta$
$Y = 2(Z + D) \tan \theta$

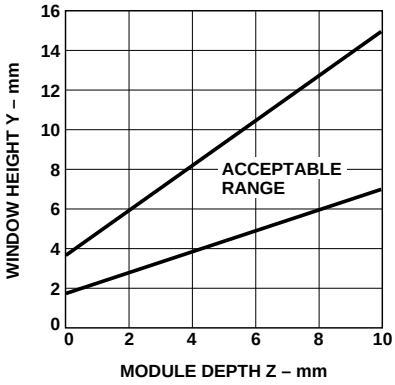
Where θ is the required half angle for viewing. For the IrDA minimum, it is 15 degrees; for the IrDA maximum, it is 30 degrees. (D is the depth of the LED image inside the part, 3.17 mm). These equations result in the following tables and graphs:

Minimum and Maximum Window Sizes

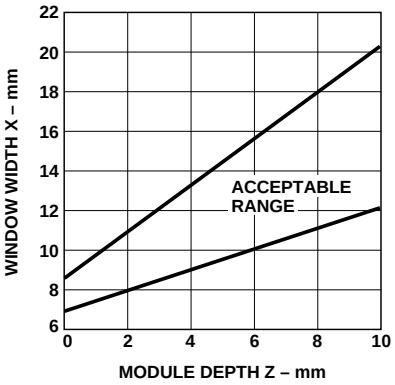
Dimensions are in mm.

Depth (Z)	Y min.	X min.	Y max.	X max.
0	1.70	6.80	3.66	8.76
1	2.23	7.33	4.82	9.92
2	2.77	7.87	5.97	11.07
3	3.31	8.41	7.12	12.22
4	3.84	8.94	8.28	13.38
5	4.38	9.48	9.43	14.53
6	4.91	10.01	10.59	15.69
7	5.45	10.55	11.74	16.84
8	5.99	11.09	12.90	18.00
9	6.52	11.62	14.05	19.15
10	7.06	12.16	15.21	20.31

Window Height Y vs. Module Depth Z



Window Width X vs. Module Depth Z



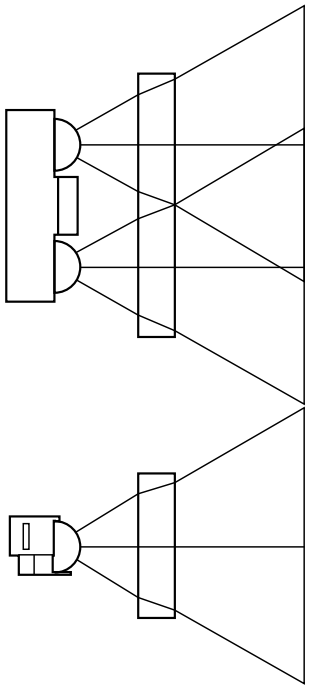
Shape of the Window

From an optics standpoint, the window should be flat. This ensures that the window will not alter either the radiation pattern of the LED, or the receive pattern of the photodiode.

If the window must be curved for mechanical design reasons, place a curve on the back side of the window that has the same radius as the front side. While this will not completely eliminate the lens effect of the front curved surface, it will reduce the effects. The amount of change in the radiation pattern is dependent upon the material chosen for the window, the radius of the front and back curves, and the distance from the back surface to the transceiver. Once these items are known, a lens design can be made which will eliminate the effect of the front surface curve.

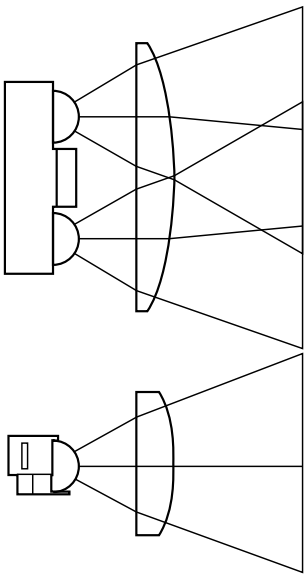
The following drawings show the effects of a curved window on the radiation pattern. In all cases, the center thickness of the window is 1.5 mm, the window is made of polycarbonate plastic, and the distance from the transceiver to the back surface of the window is 3 mm.

Flat Window



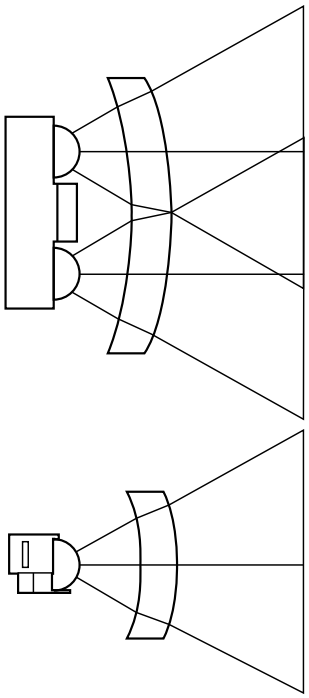
Curved Front, Flat Back

(This option is not recommended and should not be used.)



Curved Front and Back

(This option can be used if necessary for application purpose. A large radius of curvature is recommended and both front and back should have the same radius.)



Test Methods

Background Light and Electromagnetic Field

There are four ambient interference conditions in which the receiver is to operate correctly. The conditions are to be applied separately:

1. Electromagnetic Field:
   3 V/m maximum (please refer to IEC 801-3, severity level 3 for details).

2. Sunlight:
   10 kilolux maximum at the optical port. This is simulated with an IR source having a peak wavelength within the range of 850 nm to 900 nm and a spectral width of less than 50 nm biased to provide 490 $\mu W/cm^2$ (with no modulation) at the optical port. The light source faces the optical port.

   This simulates sunlight within the IrDA spectral range. The effect of longer wavelength radiation is covered by the incandescent condition.

3. Incandescent Lighting: 1000 lux maximum. This is produced with general service, tungsten-filament, gas-filled, inside frosted lamps in the 60 Watt to 100 Watt range to generate 1000 lux over the horizontal surface on which the equipment under test rests. The light sources are above the test area. The source is expected to have a filament temperature in the 2700 to 3050 Kelvin range and a spectral peak in the 850 to 1050 nm range.

4. Fluorescent Lighting:
   1000 lux maximum. This is simulated with an IR source having a peak wavelength within the range of 850 nm to 900 nm and a spectral width of less than 50 nm biased and modulated to provide an optical square wave signal (0 $\mu W/cm^2$ minimum and 0.3 $\mu W/cm^2$ peak amplitude with 10% to 90% rise and fall times less than or equal to 100 ns) over the horizontal surface on which the equipment under test rests. The light sources are above the test area. The frequency of the optical signal is swept over the frequency range from 20 kHz to 200 kHz.

   Due to the variety of fluorescent lamps and the range of IR emissions, this condition is not expected to cover all circumstances. It will provide a common floor for IrDA operation.

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